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**SOLAR CELL AND I.C. ASPECTS
OF INGOT-TO-SLICE MECHANICAL PROCESSING**

by Lawrence D. Dyer

ABSTRACT

Intensive efforts have been put into the growth of silicon crystals to suit today's solar cell and integrated circuit requirements. Each step of processing the crystal must also receive concentrated attention to preserve the grown-in perfection and to provide a suitable device-ready wafer at reasonable cost.

A comparison will be made between solar cell and I.C. requirements on the mechanical processing of silicon from ingot to wafer. Specific defects will be described that can ruin the slice or can possibly lead to device degradation. These include grinding cracks, saw exit chips, crow's-foot fractures, edge cracks, and handling scratches.

INTRODUCTION

There is abundant literature on the growth and annealing of silicon crystal ingots to provide the proper resistivity, oxygen concentration, and oxygen clustering for electronic devices. In contrast, there is less published on the mechanical processing of the ingot into slices, although this processing affects the cost and survival potential of the wafers and may affect the device quality. The purpose of the present report is to explain how certain defects can arise in ingot-to-slice processing and how they might affect either solar cells or integrated circuits.

DISCUSSION

First, some remarks will be made on the nature of mechanical processing damage and the effect of chemical etching on the resistance of the slice to breakage. Second, solar and I.C. processes will be compared in their exposure and sensitivity to damage. Third, specific defects that occur step-by-step through ingot-to-slice processing will be described and discussed. Fourth, what is needed for improvement in the mechanical processing of both solar cell and I.C. wafers will be assessed.

Nature of Damage and Effect of Chemical Etching

Mechanical damage to crystalline silicon from abrasive processes consists essentially (1,2) of two superimposed types of defects : 1) a thin layer up to 1 micron deep containing dislocations and debris, 2) microcracks up to 2 mils deep, which may have dislocation cracks extending more deeply (3,4).

Resistance of silicon to chipping or breakage during mechanical processing depends greatly on the size and sharpness of the microcracks that have been introduced. According to the Griffith formula (5,6), fracture stress depends on the inverse square root of the crack size; and, according to the Cottrell formula (7), on the square root of the ratio between tip radius and atomic radius. A calculation shows that chemical etching after an abrasive process can easily increase the resistance to fracture 100-fold.

A common misconception regarding the removal of mechanical damage is that the layer containing the damage must be removed completely. To the contrary, for crystal etching and pre-polish only enough material needs to be removed to relieve abrasion stresses and to make the wafer strong enough for further processing. This can be done with brief chemical etching which removes the dislocated region and converts any cracks to deep grooves.

Comparison of Solar and I.C. Processes

Table I shows the main steps in solar cell and I.C. mechanical processing, as well as some possible crack defects that may occur in those steps. Causes of some of these defects have been identified by the use of fracture tracing techniques (8,9). Solar cell processing has fewer steps, hence less exposure to damage. In addition, solar cell requirements are

TABLE I

STEPS IN INGOT-TO-SLICE PROCESSES vs. POSSIBLE FRACTURE DEFECTS

<u>FOR SOLAR CELLS</u>	<u>FOR INTEGRATED CIRCUITS</u>	<u>FRACTURE DEFECT</u>
CROP	CROP	LARGE CHIPS
GRIND OR SLAB	SAMPLE GRIND	SAME AS WAFERING DEFECTS
flat (opt.)	ORIENT FLAT	EXCESS CRACK DEPTH
WAFER (18 mils)	ETCH WAFER (24 mils)	EXCESS CRACK DEPTH
		EXIT CHIPS, EDGE FRACTURES DEEP MICROCRACKS, EDGE CHIPS
edge gr. (opt.)	LASER MARK EDGE GRIND HEAT TREAT LAP	CROW'S-FOOT FRACTURES EDGE CHIPPING AND CRACKS CROW'S-FOOT FRACTURES & SCRATCHES
ETCH	ETCH BACKSIDE DAMAGE POLISH	EDGE CRACKS

less severe from a cosmetic standpoint; defects such as the exit chip in sawing are not necessarily a cause for slice rejection. On the other hand, since solar cell wafers are sliced thinner than I.C. wafers, edge fractures and crow's-foot fractures are more predominant.

Specific Defects

Cropping chips.--Figure 1 shows a fracture developed from using too much blade force in a cropping saw. Silicon can be lost immediately at this work station, or the defect may not show up until the slicing stage as shown in Figure 1. This problem can obviously be solved by limiting the force.

Grinding cracks.--Figure 2 shows grinding cracks made by a centerless-type crystal grinder some years ago. The defects were found at epitaxy, where they had caused slip. Figure 3 shows schematic diagram of slip generation from excessively deep cracks formed at the crystal grinding step. Figure 4 shows grinding cracks made by a center-type crystal grinder. Clearly there is a need to limit the severity of the grinding process to minimize such cracks. One means of limiting this is provided on the Siltec crystal grinder (10), i.e. by measuring the current drawn by the drive motor (11).

Exit Chips/Saw Fractures.--Figure 5 shows a saw exit chip on a silicon slice that was made with the I.D. saw. This defect is a cosmetic one for the semiconductor industry, but a slice cannot be sold with an exit chip, partly because of potential of generating increased particle counts in the wafer fabrication facility (12). In the solar wafer the exit chip can, if severe, constitute a "saw fracture"; in fact, it is probably the major limitation on lower slice thickness for solar-cut wafers (13). The causes of exit chips have been outlined previously (14); they fall basically into two categories--bending forces (13) and wedge forces (14). Since there are numerous ways to cause the exit chip, it remains a perennial problem.

Deep Saw Damage ("Sparkle").--Figure 6 shows an area on a (100) sawed slice that reflects light preferentially at the same angle as the exit chip. This appearance is sometimes called "sparkle" and often accompanies the exit chip. The appearance is due to deeper-than-usual microcracks (14) that show up under the microscope as small, scattered facets. This collection of defects probably has one of the same causes as exit chips, but occurs earlier in the cut where the crystal still has enough breadth to resist complete crack propagation.

Saw Edge Fractures.--Figures 7 and 8 show a type of defect related to exit chips and which is cause for immediate rejection. It is a fracture that initiates at the edge and is associated with a depression in the slice caused by saw blade removal. It occurs more frequently in thin slices. Deep saw damage is often evident elsewhere on the slice. It occurs when the I.D. saw blade has lost some of its tension. On (100) slices, the cracks are parallel to saw marks; on (111) slices, they are usually

located at 30 ± 10 degrees from the exit end. The mechanism postulated for this defect is that the blade becomes too flexible, all or in part, and is deviant before entering the cut. As it enters the cut, it applies a bending stress to the wafer at its edge. In the (111) case, the mounting strip protects the edge to ± 20 deg. from the exit location. In the (100) case this protection is not enough because of the ease of making the exit chip-like fracture.

Crow's-Foot Fractures.--Figure 9 shows a schematic diagram of the edge grinding process. The wafer is held on a vacuum chuck and slowly rotated. A fast-spinning grind wheel having a groove of the desired shape is brought against the edge as shown in the cross-sections. Cooling medium is directed into the interface.

Figure 10 shows a typical crow's-foot fracture that occurred because of a 1.3-mil burr on a vacuum chuck in the edge-grind operation. Figure 11 shows the mechanism by which such fractures occur; an analysis was given previously (15). Thin slices are more susceptible to this type of fracture.

Another operation in which crow's-foot fractures originate is lapping. Note that the mechanism is different from Fig. 11; the edge-grind fracture occurs because of bending stresses, the lap fracture is thought to arise from wedging by abrasive particles (16).

Edge Cracks from Heat Treating.--Sometimes an annealing operation is carried out to stabilize resistivity. Figure 12 shows a crack formed at a slice heat treat operation. These cracks can form either from the impact of transfer into the boats or from boat slots that pinch the slice edges. In the instance of Figure 12, the temperature was high enough for dislocation generation. Such defects can also occur during fabrication of wafers into devices.

Edge Cracks at Polish.--Figures 13-14 show edge cracks that developed during the polish operation. These are characterized by nearly radial development and by polish cloth bevelling. They are envisioned to form in response to the tangential stresses that occur when the slice friction is too high and the slice edge is relatively cool.

Scratches.--Figures 15 and 16 show backside scratches that caused wafer breakages in furnace operations. The fracture origin (9) in each case coincided with the point of tangency of the scratch. This breakage is postulated to occur as follows: Furnace operations cause wafers to undergo transient stresses that bow the wafer one way or the other. If a scratch is located on the convex side of the wafer, it is subject to tensile stress which can exceed the crack propagation stress for the scratch. Such scratches must be avoided in wafer processing not only for the survival of the individual slice, but for avoiding the loss of many other devices from particles generated in the fracture process.

Improvements for Solar Cell and I.C. Mechanical Processing

Better mechanical processing methods and equipment are desired by both solar cell and I.C. industries, but the needs are divergent in some ways. Table II shows trends in slice requirements from both industries. For the electronics industry the trends dictate a broad effort to provide for larger wafer sizes, better flattening, slice identification, better edges, and smoother polishing. This means larger equipment, laser marking, and lap and polish development. For the solar cell industry the overwhelming needs are for lower cost and greater efficiency; if any gain is to be achieved in the ingot-to-slice portion, it is entirely in cost. This puts emphasis on less kerf loss, thinner slices, faster processing, etc., always with the trade-off of more chips and breakage. Increasing wafer size appears to have no benefits for solar cells because of higher I²R losses, and because the attendant increased metalization to avoid such losses causes sufficient shadowing to negate the benefit.

TABLE II
TRENDS IN SLICE REQUIREMENTS,
SOLAR AND I.C.

<u>REQUIREMENT</u>	<u>SOLAR</u>	<u>I.C.</u>
SIZE, INCHES	HOLDING AT 4-5	INCREASING TO 8
FLATNESS	O.K.	FLATTER
BOW	O.K.	LESS BOW
TRACEABILITY	--	DESIRED
LOWER COST	GREAT PRESSURE	SLIGHT PRESSURE
HIGHER QUALITY		
o EDGE	O.K.	REDUCED FRACTURES & PARTICLE GENERATION
o SURFACE	O.K.	GREATER SMOOTHNESS, NO BLEMISHES, FRONT & BACK SIDES
o INTERNAL	IMPURITY CONTROL	IMPURITY CONTROL

Considering Tables I and II together, the hopes for improvements in solar cell ingot-to-slice mechanical processing lie mainly in two areas: crop and grind and sawing. In crop and grind it is obvious that limits on sawing force and grinding drag will reduce the defects to a low level, and some benefit may be obtained from a brief crystal etch after grinding. A brief summary of possible advances in sawing for solar cells follows.

Recent advances in substrate sawing for the electronics industry have been reviewed in 1984, namely large capacity saws, slice retrieval, fault systems and productivity increasers (11). Among new features called for by users were in-situ blade tension and drag measurement. For the solar cell industry, all but the first of these advances will be useful. Unfortunately, most present equipment does not include the advances; even the blade tracking systems are mostly retrofits. Any of the new large saws may be used, but the larger blade size usually means that a thicker blade core is necessary to obtain the same stiffness, and the kerf loss is increased. The new saws may, of course, be ordered with the smaller head sizes if desired. It is the author's opinion based on the foregoing discussion that some development of new saws especially for solar cell slicing should be done, aiming more at thinner slices and thinner cuts than larger size. The following is a list of studies or developments in sawing which in the author's opinion would be of specific benefit to solar cell cost.

- o improvements in blade core strength so that thinner cores may be used.
- o in-situ blade tension measurement.
- o a method to maintain fairly constant blade tension without sacrificing blade concentricity.
- o a method of assessing the degree of damage to the slice while the slice is freshly off the saw. This would allow the operator to take corrective action before many other slices are ruined.
- o a study of why rotary crystal slicing doesn't work and the design of a saw specifically for this. This would permit smaller blades, thinner cores, and less kerf.
- o autobalancing. Silicon Technology Corporation has an autobalancing attachment, presently available for 22-inch saw heads, that does an excellent job of rebalancing the saw while running. This feature increases productivity by avoiding shutting down the saw for the imbalance that comes with broken slices, but may be a refinement that permits lower slice thicknesses.

SUMMARY

The nature of mechanical damage/chemical etching are discussed with regard to ingot-to-slice mechanical processing of solar cell and I.C. silicon material. Various examples of fracture defects are described and explained. Solar and I.C. mechanical processes are compared as well as trends in requirements in slice parameters. These considerations combine to suggest that the main area for innovative improvement in the mechanical processing of solar cell slices lies in aiming at lower cost in the wafering step. Various studies or desired features in sawing that would benefit the solar cell effort are suggested.

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REFERENCES

1. R. Stickler and G.R. Booker, *Phil. Mag.* 8(1963)859.
2. T.S. Kuan, K.K. Shih, J.A. Van Vechten and W.A. Westdorp, *J. Electrochem. Soc.*, 127(1980)1387.
3. J.W. Allen, *Phil. Mag.* 2(1957)1476.
4. J.W. Allen, *Phil. Mag.* 4(1959)1046.
5. A.A. Griffith, *Phil. Trans. Roy. Soc. London A*, 221(1921)163.
6. A.A. Griffith, *First Internat. Congr. Appl. Mech.* (Delft) (1924)55.
7. A.H. Cottrell, in "Fracture", ed. by B.L. Auerbach, D.K. Felbeck, G.T. Hahn, and D.A. Thomas, (John Wiley & Sons, New York, 1959)20.
8. L.D. Dyer, *Electrochem. Soc. Ext. Abstr.* 83-2(1983)553.
9. L.D. Dyer, "Semiconductor Processing, ASTM STP 850, Dinesh Gupta, Ed., American Society for Testing and Materials, 1984.
10. Siltec Corporation, *Product Bulletin--Model 540/590 Grinders*, Nov. 1982.
11. L.D. Dyer, *Industrial Diamond Review*, No.2, Feb. 1984, p.74.
12. L.D. Dyer, *Electrochem. Soc. Ext. Abstr.* 81-1(1981)785.
13. C.P. Chen and M.H. Leipold, *Electrochem. Soc. Ext. Abstr.* 80-2(1980)712, and *J. Electrochem. Soc.* 129(1982)2835.
14. L.D. Dyer, "Proceedings of the Low-Cost Solar Array Wafering Workshop", 8-10 June 1981, Phoenix, Ariz. Publ. No. 5101-187 DOE/JPL-1012-66.
15. L.D. Dyer and J.B. Medders, "VLSI Science and Technology/1984", ed. by K.E. Bean and G. Rozgonyi, (Electrochem. Soc., Pennington, N.J. 1984)48.
16. S. Maruyama and O. Okada, *Japan J. Appl. Phys.* 3(1964)301.

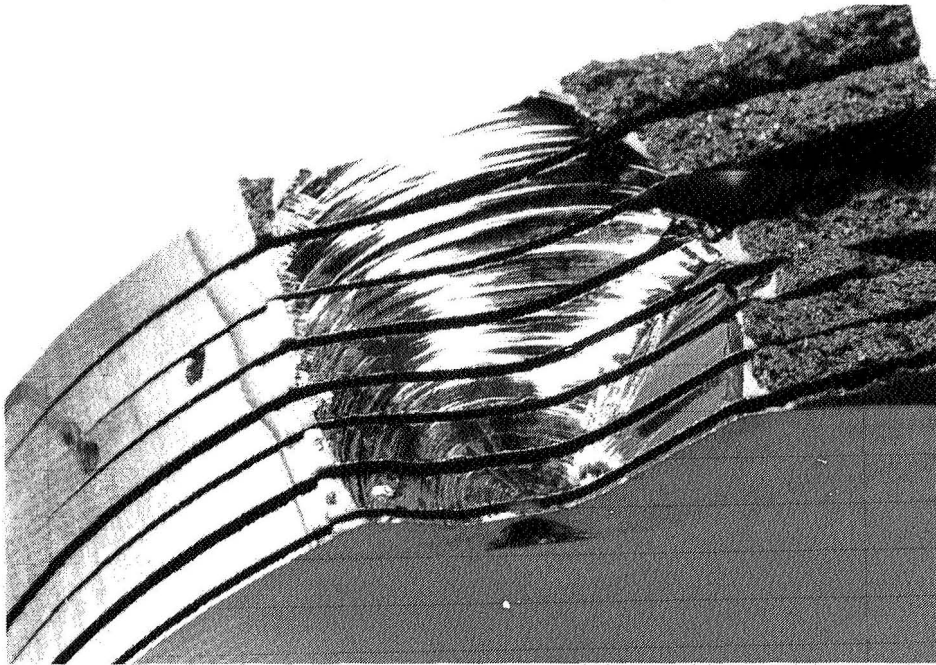


Fig. 1. Cropping chips on 100 mm silicon crystal, detected at wafering step.

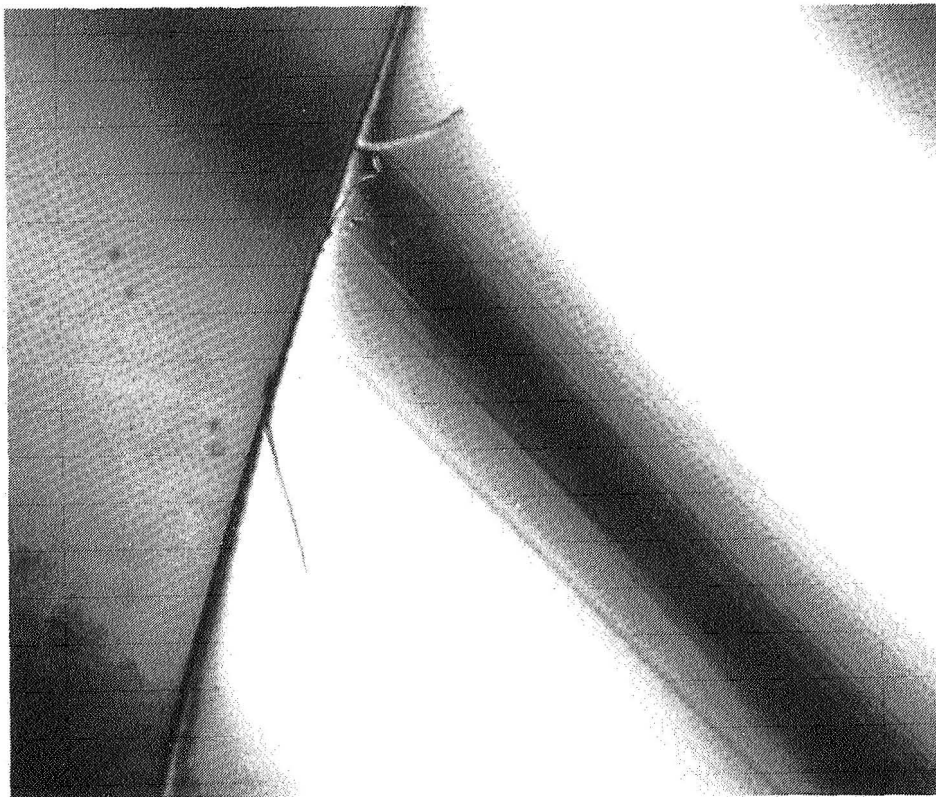
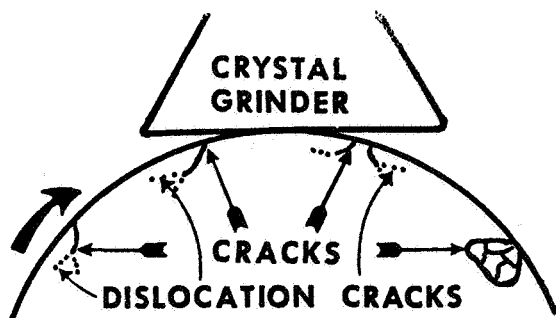
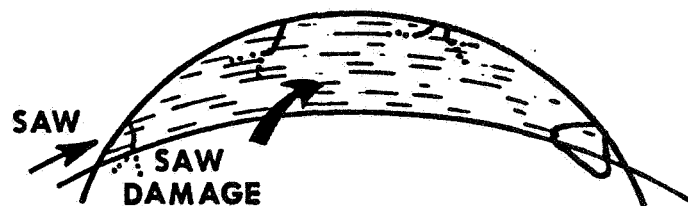


Fig. 2. Cracks produced by centerless crystal grinder and subsequent slip in epitaxial processing.



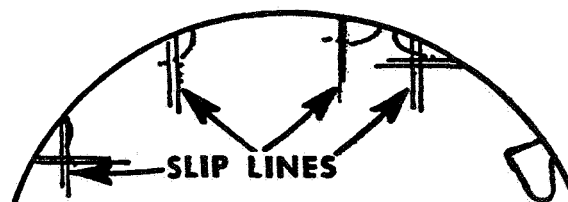
A. GRINDING OF SILICON
INGOT CAUSES CRACKS
AND DISLOCATION CRACKS.



B. SLICING PUTS IN SAW
DAMAGE AND CHIPS OUT
SOME GRINDING CAVITIES.



C. LAPPING, ETCHING AND POLISHING
REMOVES SAW DAMAGE BUT NOT ALL
OF THE GRINDING DAMAGE.



D. PROCESSING IN FURNACE OR EPI
REACTOR GENERATES SLIPLINES.

FIG. 3 SCHEMATIC OF SLIP GENERATION FROM EXCESSIVELY DEEP
CRYSTAL GRIND CRACKS.

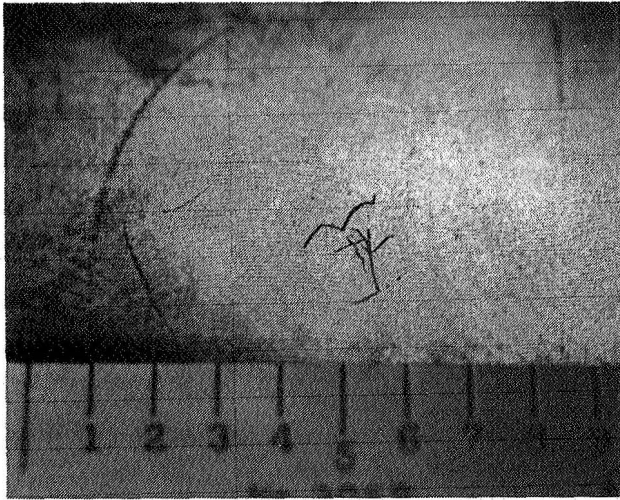


Fig. 4. Cracks produced by center-type crystal grinder.

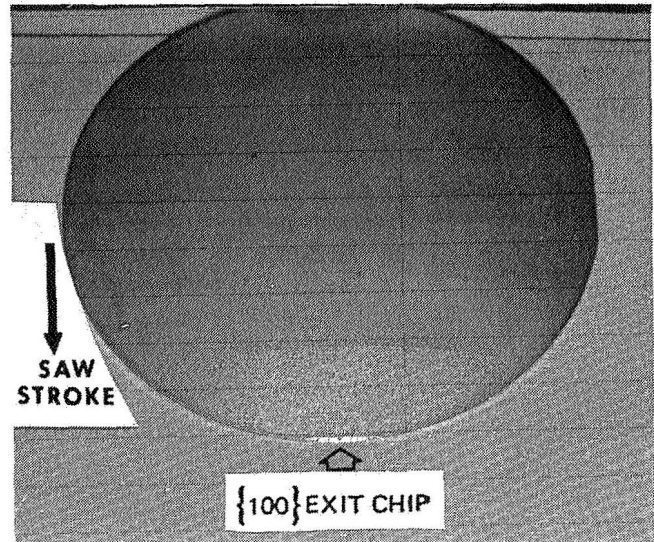


Fig. 5. Saw exit chip.

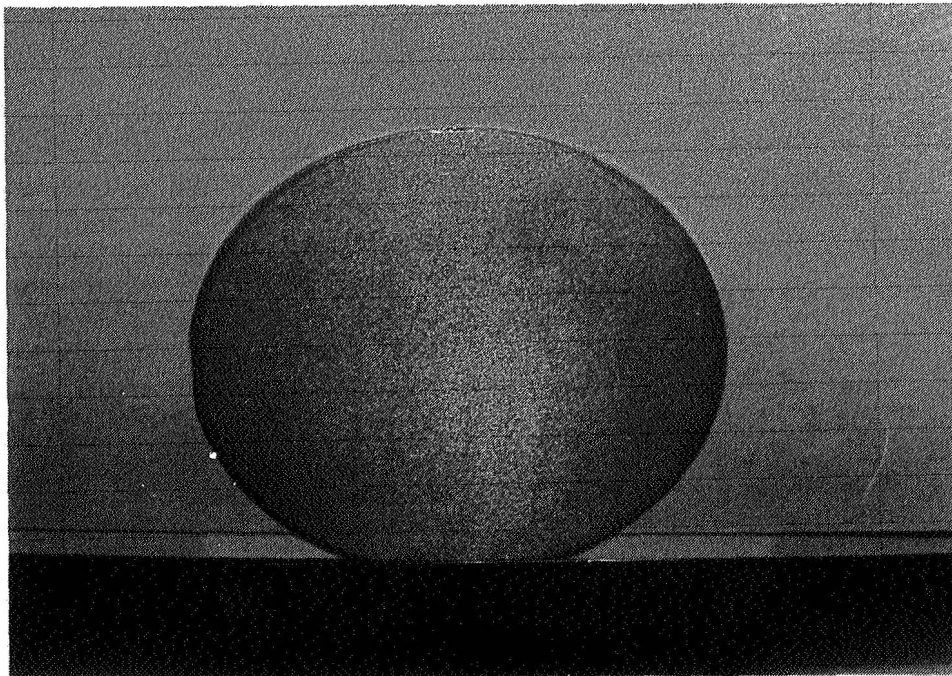


Fig. 6. Deep saw damage ("sparkle") on (100) silicon.

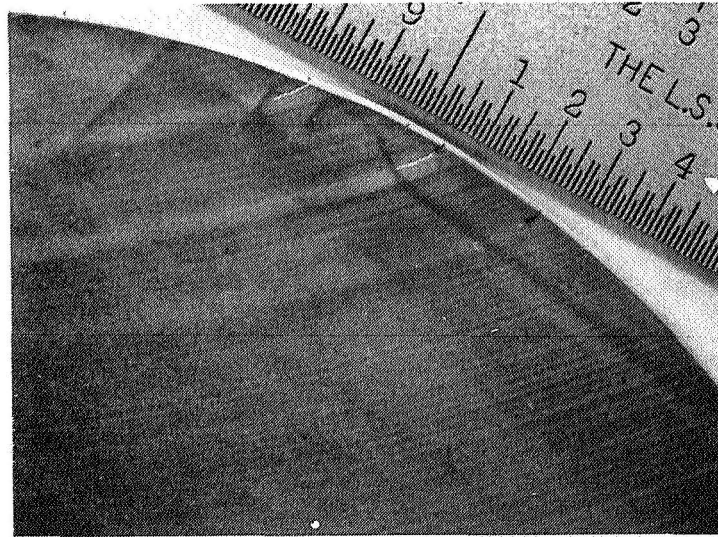


Fig. 7. Saw edge fractures--(111) silicon.

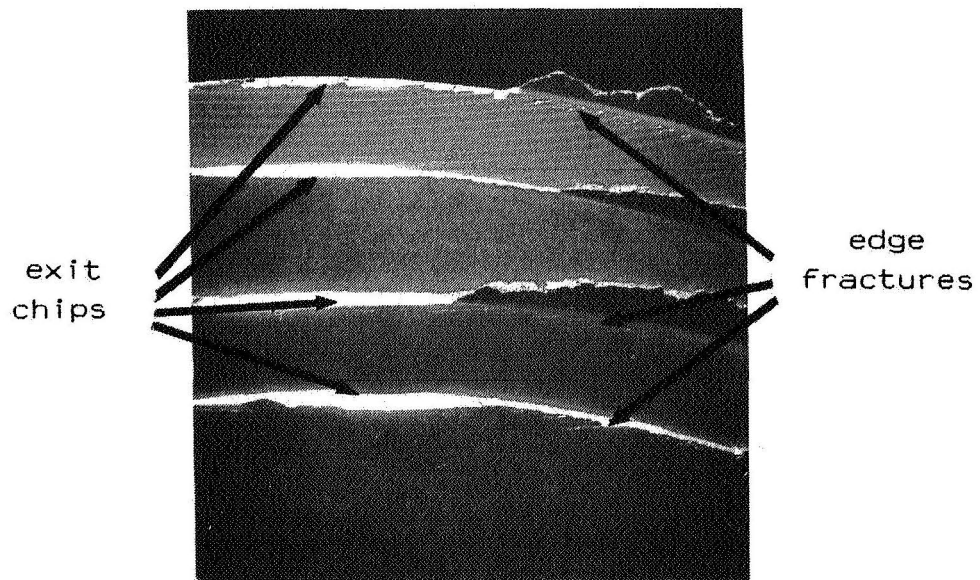


Fig. 8. Saw edge fractures--(100) silicon.

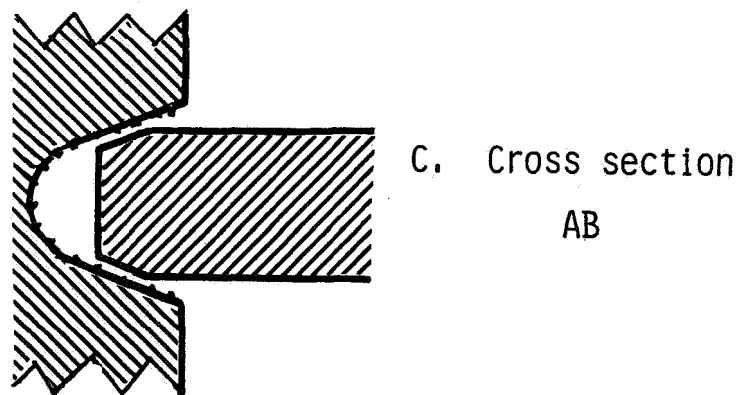
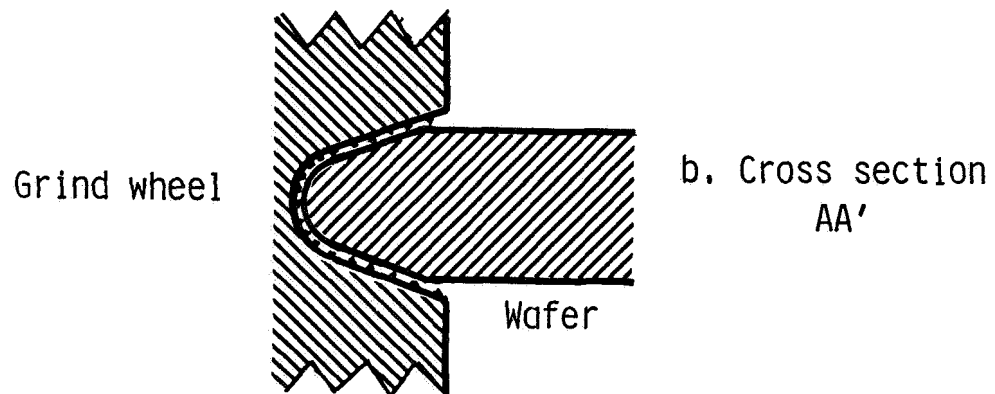
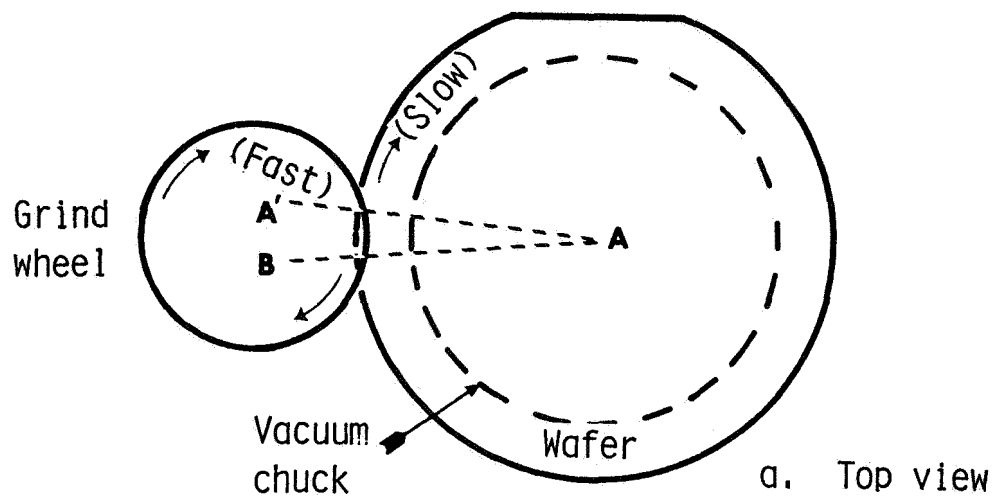


Fig. 9. Schematic Diagram of Edge Grinding Operation

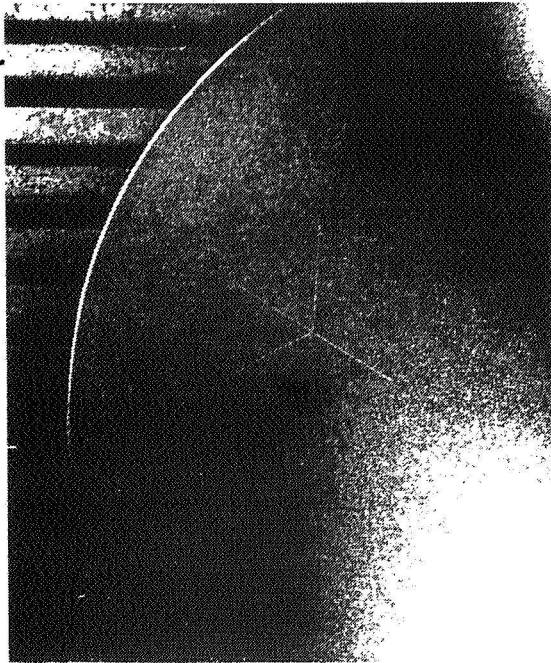


Fig. 10. Crow's-foot fracture from burr on vacuum chuck.

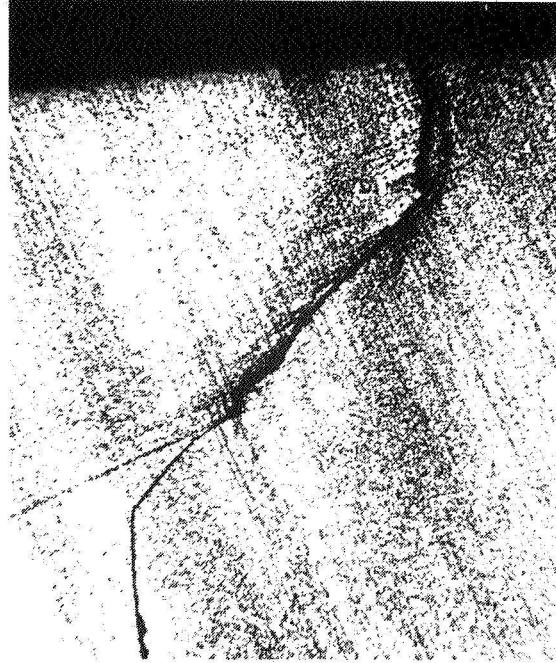


Fig. 12. Edge crack from heat-treating silicon slice in quartz boat.

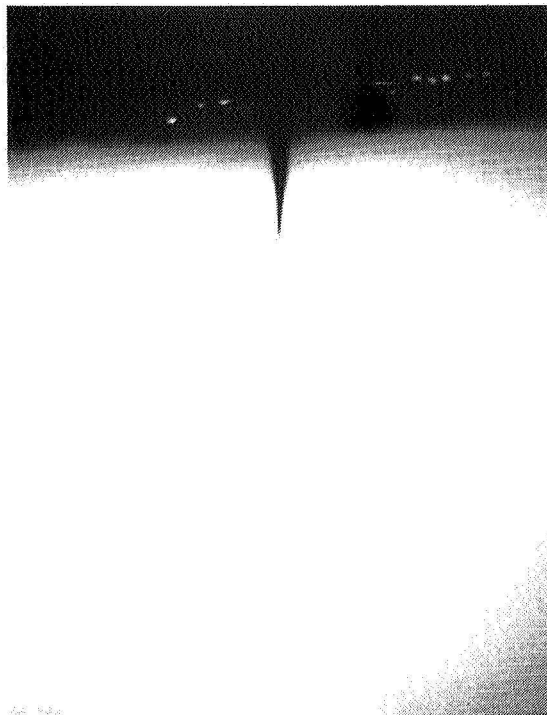
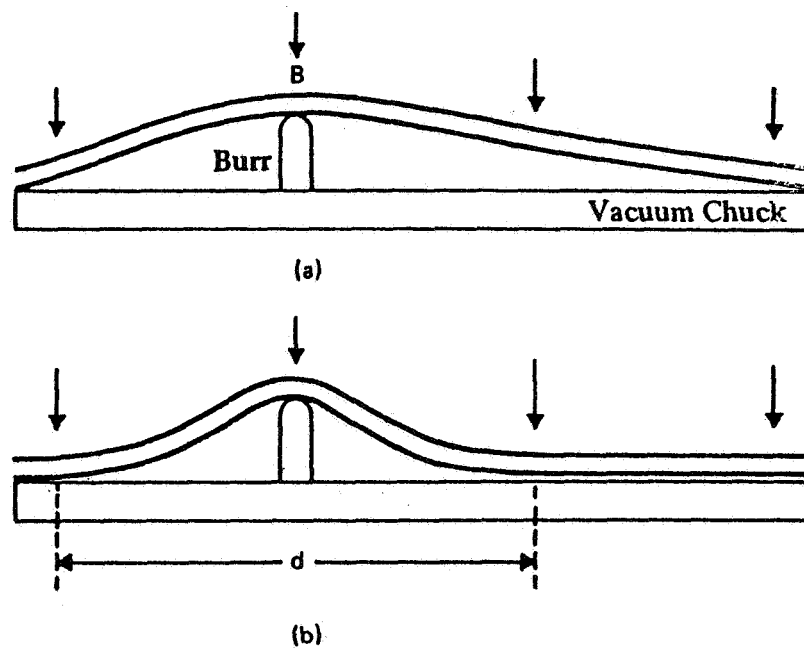


Fig. 13. Edge crack at polish.



Fig. 14. Edge crack at polish.

Fig. 11. MECHANISM OF BURR-INDUCED FRACTURE ON VACUUM CHUCK



- (a). Slice is bent over burr: max tensile stress at B. Weak vacuum
- (b). Strong vacuum flattens outer regions against plate and increases curvature and stress at 'B'.
- (c). (Not shown). Crack starts near "B" but stops as reverse curvature area is reached. (Within "d").

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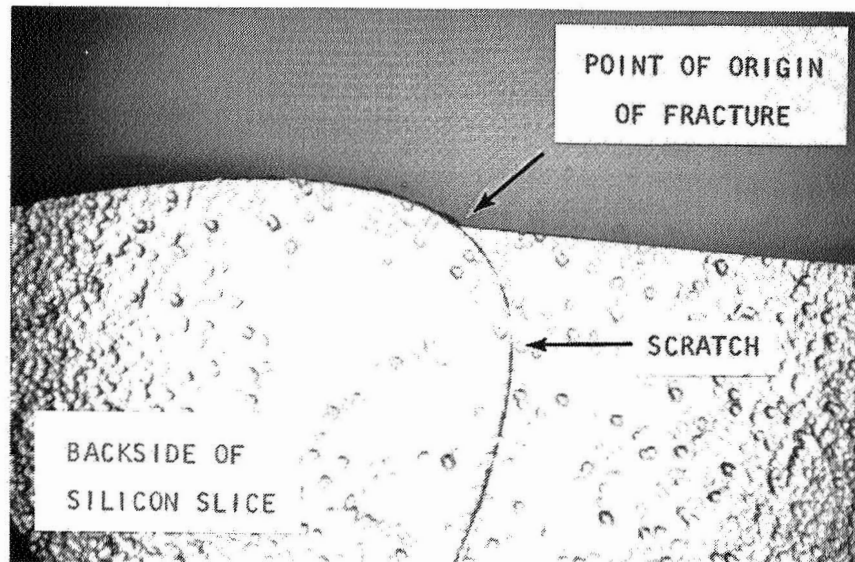


Fig. 15. Scratch leading to furnace breakage. 30X

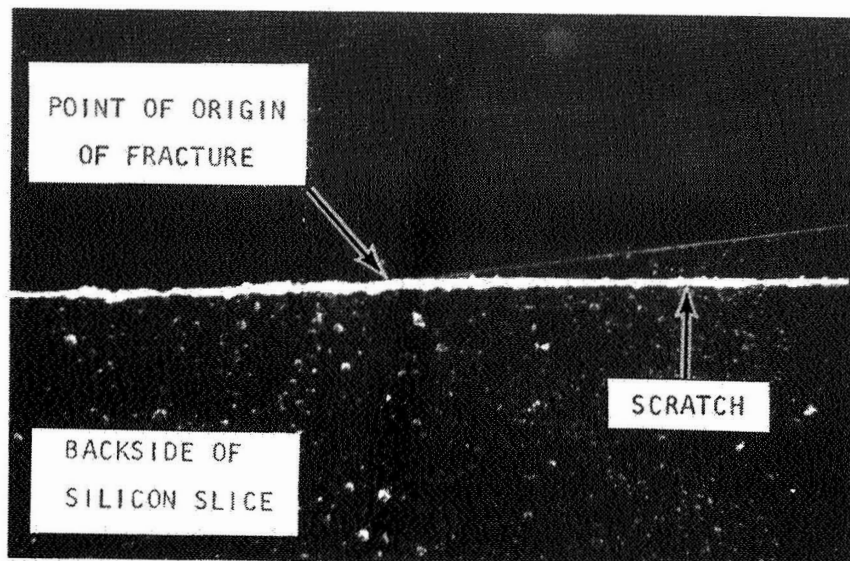


Fig. 16. Scratch leading to furnace breakage. 30X

DISCUSSION

KALEJS: What is the size of the microcracks you are talking about? Can you give us a feeling particularly of the edges versus this sparkle type of microcrack?

DYER: Normally the microcracks would be less than a mil deep. The crow's feet type of microcracks extend from 0.4 to 1.4 μm in size and average about 0.8 μm . When you get into sparkle you get much larger ones (larger than a mil).

CISZEK: It seems to me that the sawing rates that the ID saws are capable of, about 0.15 m^2/h , are hopelessly low to have the kind of throughput needed for the large photovoltaic industry. In your talk you didn't mention multiblade slurry sawing at all, and I'm wondering what your views are on that. Wacker recently demonstrated, on a pilot scale, 0.007 m^2/h per blade, which would mean a 22-blade pack would be about like an ID saw. If we really did have to get higher throughputs for photovoltaics, do you think multiblade slurry slicing is the way to go, or do you think there is some other magic solution out there, or do you think we are stuck with ID slicing?

DYER: I hope there is something better. We had a conference on this subject some years ago and at the time, multiblade sawing was not quite ready to overtake ID sawing. What bothers me about going from a 22-blade saw up to what you need to make a significant improvement is that everybody ignores the trouble it takes to get more than 22 blades on there. They talk about going to 100 or 250 or 500-blade saws, and they never mention the intensive labor to get those things all lined up, spaced properly, and so forth, and then what it would take to keep them from warping as they cut through a 6-in. slice.

LESK: If you look at sliced cast poly, you can see the grain structure very well right after slicing. Is that the sparkle effect you are talking about?

DYER: Any slice that you cut, whether poly or single-crystalline, will have a certain amount of reflection, a certain amount of preferred opening up of the cracks in crystallographic directions. I don't know whether to say that yours is the standard amount, or an enhanced amount from the presence of all the other grains, or some preferred orientation.

SCHWUTTKE: I want to answer Dr. Lesk's question of why we see the grain structure if we slice polysilicon. The fracture is orientation-dependent, and basically every grain reflects its orientation. If you look at the grain surface after fracture, you have the different cleavage planes. If you shine a point light source on it, you see light figures that can be used to orient every single grain. It is an un-isotropic hardness that is present in silicon, which is orientation-dependent, so we get different cleavage phenomena on every single orientation, and therefore after sawing you see every single grain.

- RAO: You talked about mil-deep cracks that are there after the slicing operation. If you take a slice like that and go through some sort of an acid-etching procedure, you are obviously going to blunt the tip of the crack so that crack propagation is now going to be reduced if not totally eliminated. In a case like that, one can still get fairly decent yields instead of throwing the slice out. Is that going to alleviate some of the problem?
- DYER: Yes, any etching will help solar cell processing. For integrated-circuit processing you are going to go through a lapping step first, and if you have done the etching step first, it actually hinders you because the lapping step is another controlled fracture process. You have to initiate the cracks all over again, so it doesn't buy you much there. Any time you etch it, it strengthens it.
- WOLF: With the viewpoint that you need very perfect material right up to the surface, it seems that one wants to etch everything away that has any microcracks. Then there seems to be additional bothersome evidence that the etching itself causes damage. How do we get good material right up to the surface?
- DYER: If you are going to make integrated circuits you have to polish one side, and therefore you can't end up with any blemishes at all. In fact, you use the polishing to remove the entire previously damaged area. In the in-between steps it's not necessary to take off a couple of mils on each side, as some people have said, because you are going to do that later in polishing. Dr. Schwuttke has shown that the polishing step is a more efficient step of more or less catching up with the damage. To end up with a nice surface to be able to put junctions on, and metallizations, you want to etch a little more deeply for the solar cell than you do for the integrated-circuit process. All that is necessary for the integrated-circuit process is that you enlarge the microcracks so that they are no longer cracks, but just deep grooves, until you get to the polishing stage in which you want to remove the material. We still end up with solar cells with a caustic-etched surface. There are great ups and downs, and you can still make a solar cell very well out of that without having to go to the extreme of polishing it.
- WOLF: In solar-cell manufacturing, one replaces the polishing step by an etching step to try to get rid of all the penetrating damage.
- DYER: What happens is that the grooves that you would be putting in an integrated-circuit etch have just widened out to be fairly wide cavities.
- SCHWUTTKKE: The crack tip is very sensitive to the chemical potential it sees when you do chemical etching. This is why the crack propagation or the crack removal depends very much on the etchant being used. It has been shown that safer chemical etching is actually propagating every crack. It's almost impossible by chemical etching to remove the crack tip, so this is why the modern semiconductor technique has introduced mechanical-chemical etching. Syton polishing is the most

reliable in removing cracks. You cannot remove cracks by using chemical etching because you propagate the cracks.

DYER: It may be that all chemical etching propagates cracks that are in there. Dr. Schwuttke found that for acid etches but we don't seem to find that for the caustic etches. I agree that polishing is a good way to get off that final amount of damage.

KEYACK: A couple of years ago, a lot of work was done on additives to the coolant in cutting. Can you comment on any recent work to minimize the cracks?

DYER: I'm not aware of any definitive study on the types of coolants that you add to saws. The things that have been studied were not a broad spectrum of saw coolants. The goal is not to eliminate cracks entirely, but to actually make it so that cracks form very easily, lots of them and short.